

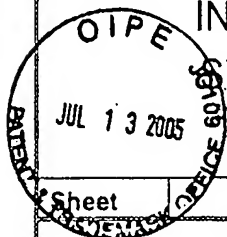
Substitute for Form 1449/PTO

Complete if Known

INFORMATION DISCLOSURE

STATEMENT BY APPLICANT

(use as many sheets as necessary)



Application Number	10/816,311
Filing Date	3/31/2003
First Named Inventor:	Nick Lindert
Art Unit	2815
Examiner Name	Nguyen, Joseph
Attorney Docket Number	42P18257

Sheet 1 of 2

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (If known)				
JN		us-	20040031979 A1	02/19/2004	Lochtefeld et al.	
		us-	6,716,684 B1	4/6/2004	Krivokapic et al.	
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		Country Code ³	Number ⁴ Kind Code ⁵ (if known)				
JN		EP	0 623 963 A1	11/9/1994	Siemens AG		
JN		WO	02/43151A	5/30/2002	Hitachi ULSI Sys Co Ltd		

 Examiner
Signature

JOSEPH NGUYEN

Date Considered

9/13/05

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Sheet	2	42P18257	2	Attorney Docket Number	42P18257
NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			T ²
JN		T. Park et al., "Fabrication of Body-Tied FinFETs (Omega MOSFETS) Using Bulk Si Wafers", 2003 Symposia on VLSI Technology Digest of Technical Papers, June 2003, pages 135-136.			
		V. Subramanian et al., "A Bulk-Si-Compatible Ultrathin-body SOI Technology for Sub-100m MOSFETS" Proceeding of the 57th Annual Device Research Conference, pp. 28-29 (1999)			
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		Hisamoto, Digh et al. "FinFET- A Self-Aligned Double-Gate MOSFET Scalable to 20 nm", IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325			
		International Search Report PCT/US 03/26242			
		International Search Report PCT/US 03/39727			
		International Search Report PCT/US 03/40320			

Examiner Signature	JOSEPH NGUYEN	Date Considered	9/13/05
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